The equations of the ideal latches

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Abstract. The latches are simple circuits with feedback from the digital electrical engineering. We have included in our work the C element of Muller, the RS latch, the clocked RS latch, the D latch and also circuits containing two interconnected latches: the edge triggered RS flip-flop, the D flip-flop, the JK flip-flop, the T flip-flop. The purpose of this study is to model with equations the previous circuits, considered to be ideal, i.e. non-inertial. The technique of analysis is the pseudoboolean differential calculus.
Keywords: latch, flip-flop, pseudo-boolean equations.

1 Latches, the general equation

$\mathbf{B} = \{0, 1\}$ is the Boole algebra with two elements. The (normal) signals are by definition the functions $x : \mathbf{R} \longrightarrow \mathbf{B}$ of the form

$$x(t) = x(\tau_0 - 0) \cdot \varphi_{(-\infty,\tau_0)}(t) \oplus x(\tau_0) \cdot \varphi_{[\tau_0,\tau_1)}(t) \oplus x(\tau_1) \cdot \varphi_{[\tau_1,\tau_2)}(t) \oplus ...$$

where $\mathbf{R}$ is the time set, $\varphi_{()} : \mathbf{R} \to \mathbf{B}$ is the characteristic function and $0 \leq \tau_0 < \tau_1 < \tau_2 < ...$ is an unbounded sequence. The equations of the (ideal) latches consist in the next system

$$\begin{cases} \overline{x(t-0)} \cdot x(t) = \overline{x(t-0)} \cdot u(t) \\ x(t-0) \cdot \overline{x(t)} = x(t-0) \cdot v(t) \\ u(t) \cdot v(t) = 0 \end{cases} \tag{1.1}$$

where u, v, x are signals and x is the unknown. The last equation of the system is called the admissibility condition (of the inputs). In order to solve the system (1.1) we associate to the functions u, v the next sets U_{2k}, V_{2k+1}

and respectively numbers t_k:

$$\begin{array}{rcll} U_0 & = & \{t|\overline{u(t-0)}\cdot u(t)=1\}, & t_0=\min U_0 \\ V_1 & = & \{t|\overline{v(t-0)}\cdot v(t)=1, t>t_0\}, & t_1=\min V_1 \\ U_2 & = & \{t|\overline{u(t-0)}\cdot u(t)=1, t>t_1\}, & t_2=\min U_2 \\ V_3 & = & \{t|\overline{v(t-0)}\cdot v(t)=1, t>t_2\}, & t_3=\min V_3 \\ & & ... & \end{array}$$

and the next inclusions, respectively inequalities are true:

$$U_0 \supset U_2 \supset U_4 \supset ... \quad V_1 \supset V_3 \supset V_5 \supset ...$$

$$0 \leq t_0 < t_1 < t_2 < ...$$

For each of U_{2k} (V_{2k+1}) we have the possibilities:

- it is empty. Then t_{2k} (t_{2k+1}) is undefined and all U_{2k}, V_{2k+1}, t_k of higher rank are undefined

- it is non-empty, finite or infinite. t_{2k} (t_{2k+1}) is defined

If U_{2k} (V_{2k+1}) are defined for all $k \in \mathbf{N}$, then the sequence (t_k) is unbounded.

A similar discussion is related with the sets V'_{2k}, U'_{2k+1} and respectively numbers t'_k :

$$\begin{array}{rcll} V'_0 & = & \{t|\overline{v(t-0)}\cdot v(t)=1\}, & t'_0=\min V'_0 \\ U'_1 & = & \{t|\overline{u(t-0)}\cdot u(t)=1, t>t'_0\}, & t'_1=\min U'_1 \\ V'_2 & = & \{t|\overline{v(t-0)}\cdot v(t)=1, t>t'_1\}, & t'_2=\min V'_2 \\ U'_3 & = & \{t|\overline{u(t-0)}\cdot u(t)=1, t>t'_2\}, & t'_3=\min U'_3 \\ & & ... & \end{array}$$

For solving the system (1.1) we observe that the unbounded sequence $0 \leq t''_0 < t''_1 < t''_2 < ...$ exists with the property that u, v, x are constant in each of the intervals $(-\infty, t''_0), [t''_0, t''_1), [t''_1, t''_2), ...$ where the first two equations of (1.1) take one of the forms

$$\left\{ \begin{array}{c} \overline{x(t-0)}\cdot x(t)=\overline{x(t-0)} \\ x(t-0)\cdot \overline{x(t)}=0 \end{array} \right. \tag{1.2}$$

$$\left\{ \begin{array}{c} \overline{x(t-0)}\cdot x(t)=0 \\ x(t-0)\cdot \overline{x(t)}=x(t-0) \end{array} \right. \tag{1.3}$$

$$\left\{ \begin{array}{c} \overline{x(t-0)}\cdot x(t)=0 \\ x(t-0)\cdot \overline{x(t)}=0 \end{array} \right. \tag{1.4}$$

as $u(t), v(t)$ are equal with $1,0;0,1;0,0$ in those intervals. The solutions were written in the next table

	$eq \quad (1.2)$	$eq \quad (1.3)$	$eq \quad (1.4)$
	$u(t)=1, v(t)=0$	$u(t)=0, v(t)=1$	$u(t)=v(t)=0$
$t \in (-\infty, t_0^{"})$	$x(t)=1$	$x(t)=0$	$x(t)=0$ $x(t)=1$
$t \in [t_k^{"}, t_{k+1}^{"})$	$x(t)=1$	$x(t)=0$	$x(t)=x(t_k^{"}-0)$

Table 1

Theorem Equation (1.1) is equivalent with the equation

$$x(t) \cdot u(t) \cdot \overline{v(t)} \cup \overline{x(t)} \cdot \overline{u(t)} \cdot v(t) \cup \tag{1.5}$$

$$\cup (\overline{x(t-0)} \cdot \overline{x(t)} \cup x(t-0) \cdot x(t)) \cdot \overline{u(t)} \cdot \overline{v(t)} = 1$$

Proof The proof is elementary and it is omitted.

Equation (1.5) contains three exclusive possibilities: $x(t) \cdot u(t) \cdot \overline{v(t)} = 1$, $\overline{x(t)} \cdot \overline{u(t)} \cdot v(t) = 1$, respectively $(\overline{x(t-0)} \cdot \overline{x(t)} \cup x(t-0) \cdot x(t)) \cdot \overline{u(t)} \cdot \overline{v(t)} = 1$ equivalent with (1.2), (1.3), (1.4).

We solve the system (1.1).

Case a) $u(0-0)=0, v(0-0)=0$

$x(0-0)=0$ and $x(0-0)=1$ are both possible. In order to make a distinction between the two solutions of (1.1) corresponding to the initial value 0, respectively to the initial value 1 we shall note them with x, respectively with x'.

a.i) $x(0-0)=0$

a.i.1) $U_0 = \emptyset$

the solution of (1.1) is $x(t)=0$

a.i.2) $U_0 \neq \emptyset$

and $\exists \varepsilon > 0, x(t) = \varphi_{[t_0,\infty)}(t)$ for $t < t_0 + \varepsilon$. This fact results by solving (1.4) for $t < t_0$ and then (1.2) followed perhaps by a finite sequence of (1.4), (1.2), (1.4),... in some interval $[t_0, t_0+\varepsilon)$. Furthermore

a.i.2.1) $V_1 = \emptyset$

the solution of (1.1) is $x(t) = \varphi_{[t_0,\infty)}(t)$.

a.i.2.2) $V_1 \neq \emptyset$

and $\exists \varepsilon > 0, x(t) = \varphi_{[t_0,t_1)}(t)$ for $t < t_1 + \varepsilon$. In some interval $[t_1, t_1+\varepsilon)$, we solved (1.3) followed perhaps by a finite sequence of (1.4), (1.3), (1.4),...

a.i.2.2.1) $U_2 = \emptyset$

the solution of (1.1) is $x(t) = \varphi_{[t_0,t_1)}(t)$

a.i.2.2.2) $U_2 \neq \emptyset$

and $\exists \varepsilon > 0, x(t) = \varphi_{[t_0,t_1)}(t) \oplus \varphi_{[t_2,\infty)}(t)$ for $t < t_2 + \varepsilon$.

a.i.2.2.2.1) $V_3 = \emptyset$

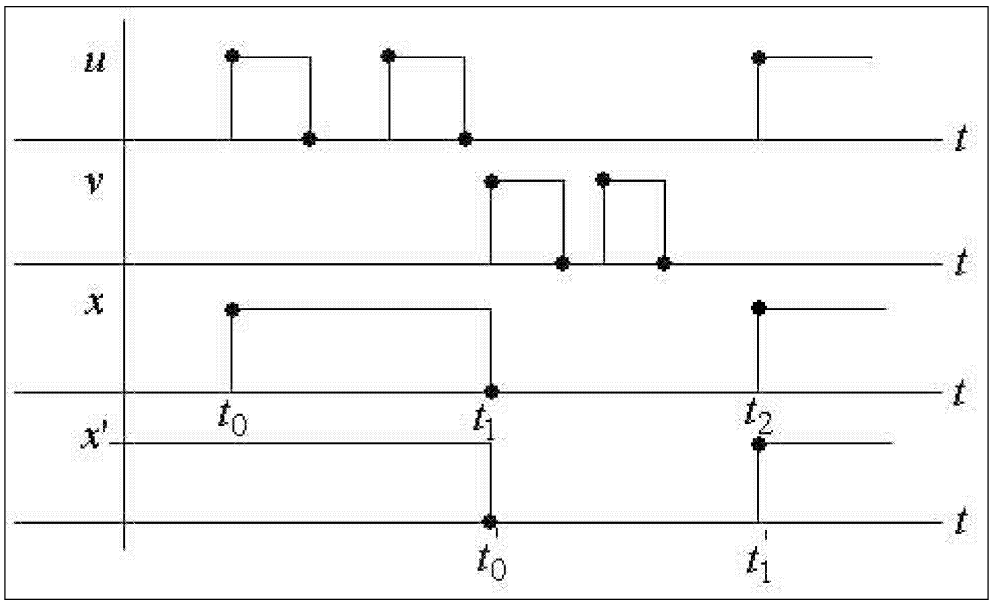

Figure 1: Case a), $t_0 < t_0'$

the solution of (1.1) is $x(t) = \varphi_{[t_0,t_1)}(t) \oplus \varphi_{[t_2,\infty)}(t)$
a.i.2.2.2.2) $V_3 \neq \emptyset$
...
a.ii) $x'(0-0) = 1$
a.ii.1) $V_0' = \emptyset$
the solution of (1.1) is $x'(t) = 1$
a.ii.2) $V_0' \neq \emptyset$
$\exists \varepsilon > 0, x'(t) = \varphi_{(-\infty,t_0')}(t)$ for all $t < t_0' + \varepsilon$
a.ii.2.1) $U_1' = \emptyset$
the solution of (1.1) is $x'(t) = \varphi_{(-\infty,t_0')}(t)$
a.ii.2.2) $U_1' \neq \emptyset$
$\exists \varepsilon > 0, x'(t) = \varphi_{(-\infty,t_0')}(t) \oplus \varphi_{[t_1',\infty)}(t)$ for all $t < t_1' + \varepsilon$
...

We have drawn in Figures 1 and 2 the solutions x, x' corresponding to Case a) in the situation when $t_0 < t_0'$, respectively when $t_0 > t_0'$ (the equality $t_0 = t_0'$ is impossible, because it implies $u(t_0) = v(t_0') = 1$, contradiction with (1.1)). We observe the fact that $x_{|[t_0,\infty)} = x'_{|[t_0,\infty)}$, respectively $x_{|[t_0',\infty)} = x'_{|[t_0',\infty)}$ thus after the first common value of the (distinct) solutions x, x' they coincide.

Case b) $u(0-0) = 1, v(0-0) = 0$
the only possibility is $x(0-0) = 1$

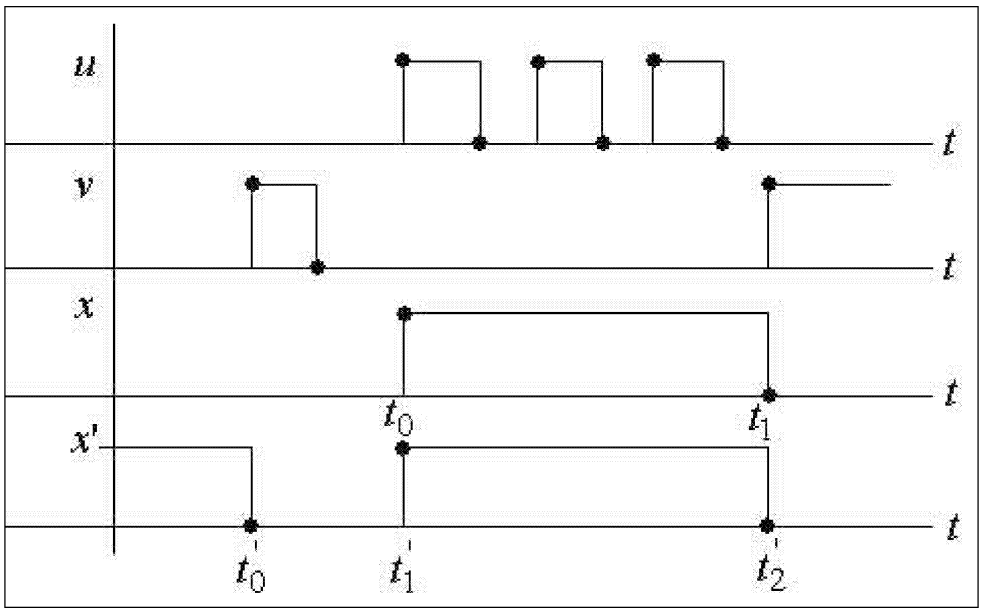

Figure 2: Case a), $t_0 > t_0'$

b.1) $V_0' = \emptyset$
the solution of (1.1) is $x(t) = 1$
b.2) $V_0' \neq \emptyset$
$\exists \varepsilon > 0, x(t) = \varphi_{(-\infty, t_0')}(t)$ for all $t < t_0' + \varepsilon$
...
Case c) $u(0-0) = 0, v(0-0) = 1$
the only possibility is $x(0-0) = 0$
c.1) $U_0 = \emptyset$
the solution of (1.1) is $x(t) = 0$
c.2) $U_0 \neq \emptyset$
$\exists \varepsilon > 0, x(t) = \varphi_{[t_0, \infty)}(t)$ for $t < t_0 + \varepsilon$
...
We have proved the next

Theorem If $u(t) = v(t) = 0$, the system (1.1) has two solutions $x(t) = 0$ and $x(t) = 1$. If $u(0-0) = v(0-0) = 0$ but $\exists t > 0, u(t) \cup v(t) = 1$, then (1.1) has two distinct solutions corresponding to $x(0-0) = 0$ and $x(0-0) = 1$, that become equal at the first time instant $t > 0$ when $u(t) \cup v(t) = 1$. And if $u(0-0) \cup v(0-0) = 1$, then the solution is unique.

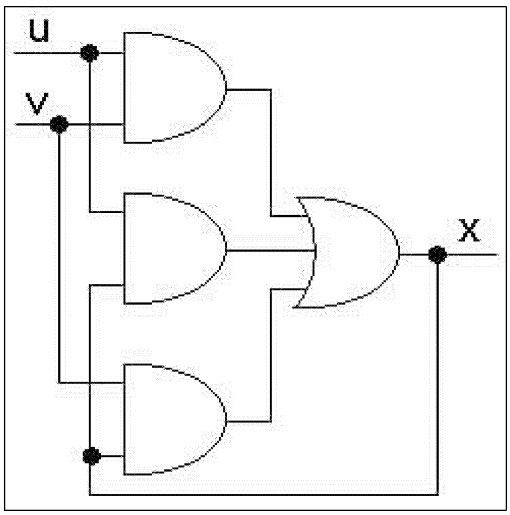

Figure 3: The C element of Muller

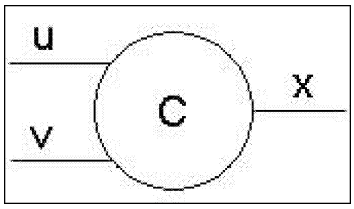

Figure 4: The symbol of the C element of Muller

2 C element

We call the equations of the C element of Muller any of the next equivalent statements:

$$\begin{cases} \overline{x(t-0)} \cdot x(t) = \overline{x(t-0)} \cdot u(t) \cdot v(t) \\ x(t-0) \cdot \overline{x(t)} = x(t-0) \cdot \overline{u(t)} \cdot \overline{v(t)} \end{cases} \tag{2.1}$$

and respectively

$$x(t) \cdot u(t) \cdot v(t) \cup \overline{x(t)} \cdot \overline{u(t)} \cdot \overline{v(t)} \cup \tag{2.2}$$
$$\cup (\overline{x(t-0)} \cdot \overline{x(t)} \cup x(t-0) \cdot x(t)) \cdot (\overline{u(t)} \cdot v(t) \cup u(t) \cdot \overline{v(t)}) = 1$$

where u, v, x are signals, the first two called inputs and the last – state. Equations (2.1), (2.2) are the equations of a latch (1.1), (1.5) where $u(t)$ is replaced by $u(t) \cdot v(t)$ and $v(t)$ is replaced by $\overline{u(t)} \cdot \overline{v(t)}$. It is observed the satisfaction of the admissibility condition of the inputs. The analysis of (2.2) is obvious: $x(t)$ is 1 if $u(t) = v(t) = 1$, $x(t)$ is 0 if $u(t) = v(t) = 0$ and

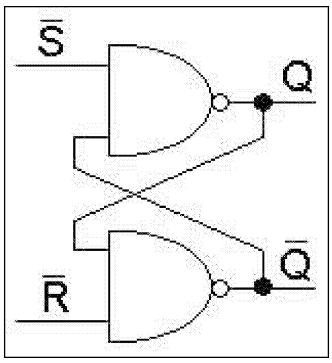

Figure 5: The RS latch circuit

$x(t) = x(t-0)$, $x(t)$ keeps its previous value otherwise. The general form of equations (2.1), (2.2) for m inputs $u_1, ..., u_m$ is

$$\begin{cases} \overline{x(t-0)} \cdot x(t) = \overline{x(t-0)} \cdot u_1(t) \cdot ... \cdot u_m(t) \\ x(t-0) \cdot \overline{x(t)} = x(t-0) \cdot \overline{u_1(t)} \cdot ... \cdot \overline{u_m(t)} \end{cases}$$

$$x(t) \cdot u_1(t) \cdot ... \cdot u_m(t) \cup \overline{x(t)} \cdot \overline{u_1(t)} \cdot ... \cdot \overline{u_m(t)} \cup$$
$$\cup (\overline{x(t-0)} \cdot \overline{x(t)} \cup x(t-0) \cdot x(t)) \cdot \overline{u_1(t) \cdot ... \cdot u_m(t)} \cdot (u_1(t) \cup ... \cup u_m(t)) = 1$$

3 RS latch

The equations of the RS latch are given by

$$\begin{cases} \overline{Q(t-0)} \cdot Q(t) = \overline{Q(t-0)} \cdot S(t) \\ Q(t-0) \cdot \overline{Q(t)} = Q(t-0) \cdot R(t) \\ R(t) \cdot S(t) = 0 \end{cases} \tag{3.1}$$

and equivalently by

$$Q(t) \cdot \overline{R(t)} \cdot S(t) \cup \overline{Q(t)} \cdot R(t) \cdot \overline{S(t)} \cup \tag{3.2}$$
$$\cup (\overline{Q(t-0)} \cdot \overline{Q(t)} \cup Q(t-0) \cdot Q(t)) \cdot \overline{R(t)} \cdot \overline{S(t)} = 1$$

In (3.1), (3.2) R, S, Q are signals. R, S are called inputs: the reset input and the set input and Q is the state, the unknown relative to which the equations are solved. These equations coincide with (1.1) and (1.5) but the notations are different and traditional. We conclude the things that were discussed in section 1 by the next statements related with equation (3.2). At the RS latch, $Q(t) = 1$ if $R(t) = 0, S(t) = 1$; $Q(t) = 0$ if $R(t) = 1, S(t) = 0$; and $Q(t) = Q(t-0), Q$ keeps its previous value if $R(t) = 0, S(t) = 0$.

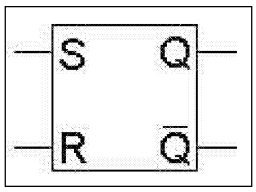

Figure 6: The symbol of the RS latch

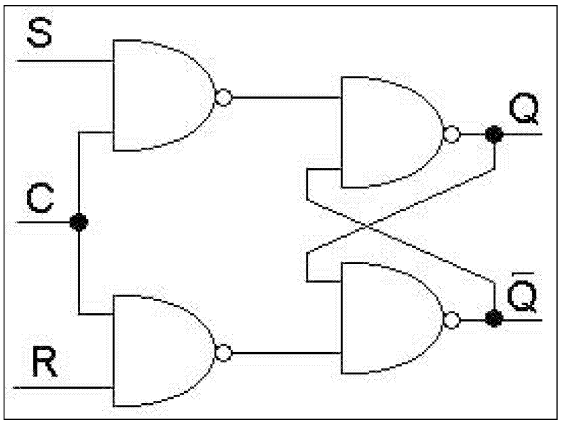

Figure 7: The clocked RS latch circuit

4 Clocked RS latch

The equivalent statements

$$\begin{cases} \overline{Q(t-0)} \cdot Q(t) = \overline{Q(t-0)} \cdot S(t) \cdot C(t) \\ Q(t-0) \cdot \overline{Q(t)} = Q(t-0) \cdot R(t) \cdot C(t) \\ R(t) \cdot S(t) \cdot C(t) = 0 \end{cases} \tag{4.1}$$

and

$$\begin{gathered} C(t) \cdot (Q(t) \cdot \overline{R(t)} \cdot S(t) \cup \overline{Q(t)} \cdot R(t) \cdot \overline{S(t)} \cup \\ \cup (\overline{Q(t-0)} \cdot \overline{Q(t)} \cup Q(t-0) \cdot Q(t)) \cdot \overline{R(t)} \cdot \overline{S(t)}) \cup \\ \cup \overline{C(t)} \cdot (\overline{Q(t-0)} \cdot \overline{Q(t)} \cup Q(t-0) \cdot Q(t)) = 1 \end{gathered} \tag{4.2}$$

are called the equations of the clocked RS latch. R, S, C, Q are signals:. the reset, the set and the clock input, respectively the state. The equations (4.1), (4.2) result from (1.1) and (1.5) where $u(t) = S(t) \cdot C(t)$, $v(t) = R(t) \cdot C(t)$. The clocked RS latch behaves like an RS latch when $C(t) = 1$ and keeps the state constant $Q(t) = Q(t-0)$ when $C(t) = 0$.

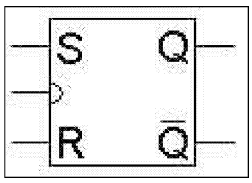

Figure 8: The symbol of the clocked RS latch

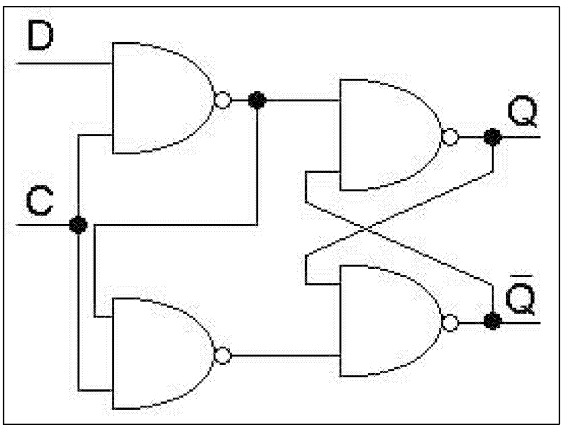

Figure 9: The D latch circuit

5 D latch

We call the equations of the D latch any of the next equivalent statements

$$\begin{cases} \overline{Q(t-0)} \cdot Q(t) = \overline{Q(t-0)} \cdot D(t) \cdot C(t) \\ Q(t-0) \cdot \overline{Q(t)} = Q(t-0) \cdot \overline{D(t)} \cdot C(t) \end{cases} \tag{5.1}$$

and respectively

$$C(t) \cdot (\overline{Q(t)} \cdot \overline{D(t)} \cup Q(t) \cdot D(t)) \cup \overline{C(t)} \cdot (\overline{Q(t-0)} \cdot \overline{Q(t)} \cup Q(t-0) \cdot Q(t)) = 1 \tag{5.2}$$

D, C, Q are signals: the data input D, the clock input C and the state Q. On one hand, from (5.1) it is seen the satisfaction of the admissibility condition of the inputs. And on the other hand (5.1), (5.2) result from the equations of the clocked RS latch (4.1), (4.2) where $R = \overline{S \cdot C}$ and we have used the traditional notation D for the data input, instead of S. When $C(t) = 1$, the D latch makes $Q(t) = D(t)$ and when $C(t) = 0$, Q is constant.

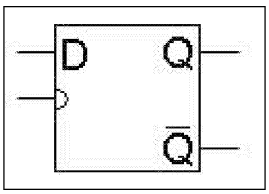

Figure 10: The symbol of the D latch

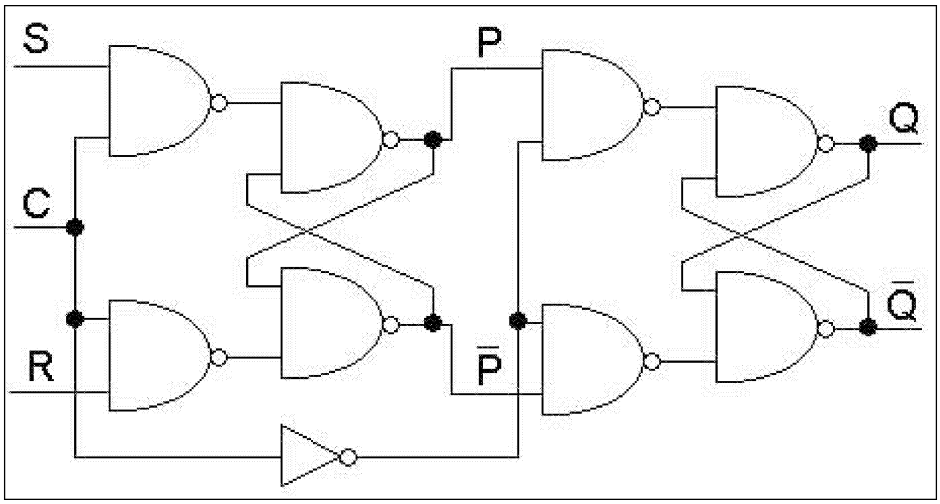

Figure 11: The edge triggered RS flip-flop circuit

6 Edge triggered RS flip-flop

Any of the equivalent statements

$$\begin{cases} \overline{P(t-0)} \cdot P(t) = \overline{P(t-0)} \cdot S(t) \cdot C(t) \\ P(t-0) \cdot \overline{P(t)} = P(t-0) \cdot R(t) \cdot C(t) \\ R(t) \cdot S(t) \cdot C(t) = 1 \\ \overline{Q(t-0)} \cdot Q(t) = \overline{Q(t-0)} \cdot P(t) \cdot \overline{C(t)} \\ Q(t-0) \cdot \overline{Q(t)} = Q(t-0) \cdot \overline{P(t)} \cdot \overline{C(t)} \end{cases} \tag{6.1}$$

and respectively

$$\begin{gathered} C(t) \cdot (\overline{Q(t-0)} \cdot \overline{Q(t)} \cup Q(t-0) \cdot Q(t)) \cdot (P(t) \cdot \overline{R(t)} \cdot S(t) \cup \\ \cup \overline{P(t)} \cdot R(t) \cdot \overline{S(t)} \cup (\overline{P(t-0)} \cdot \overline{P(t)} \cup P(t-0) \cdot P(t)) \cdot \overline{R(t)} \cdot \overline{S(t)}) \cup \\ \cup \overline{C(t)} \cdot (\overline{Q(t)} \cdot \overline{P(t-0)} \cdot \overline{P(t)} \cup Q(t) \cdot P(t-0) \cdot P(t)) = 1 \end{gathered} \tag{6.2}$$

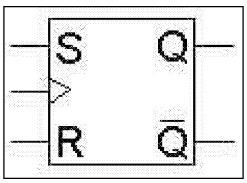

Figure 12: The symbol of the edge triggered RS flip-flop

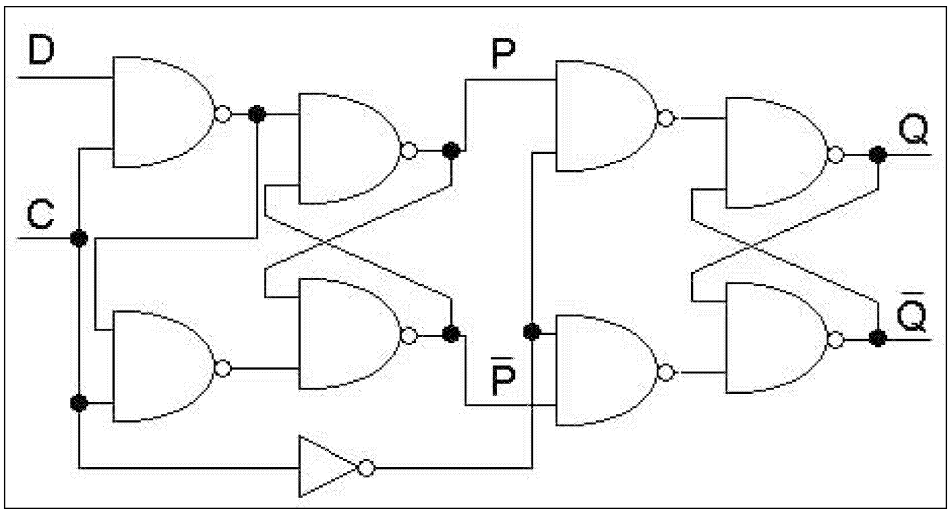

Figure 13: The D flip-flop circuit

is called the equation of the edge triggered RS flip-flop. R, S, C, P, Q are signals: the reset input R, the set input S, the clock input C, the next state P and the state Q. In (6.1), (6.2) the signals R, S, C, P and $P, \overline{C}, Q$ satisfy the equations of a clocked RS latch and of a D latch and (6.2) represents the term by term product of (4.2) with (5.2) written with these variables. The two latches are called master and slave. The name of edge triggered RS flip-flop refers to the fact that $Q(t)$ is constant at all time instances except $C(t-0) \cdot \overline{C(t)} = 1$, when $Q(t) = P(t-0) = \begin{cases} 1, if & R(t-0) = 0, S(t-0) = 1 \\ 0, if & R(t-0) = 1, S(t-0) = 0 \end{cases}$, this is the so called 'falling edge' of the clock input.

7 D flip-flop

We call the equations of the D flip-flop any of the next equivalent conditions:

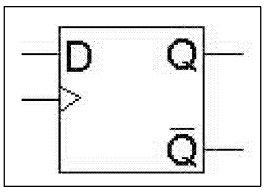

Figure 14: The symbol of the D flip-flop

$$\begin{cases} \overline{P(t-0)} \cdot P(t) = \overline{P(t-0)} \cdot D(t) \cdot C(t) \\ P(t-0) \cdot \overline{P(t)} = P(t-0) \cdot \overline{D(t)} \cdot C(t) \\ \overline{Q(t-0)} \cdot Q(t) = \overline{Q(t-0)} \cdot P(t) \cdot \overline{C(t)} \\ Q(t-0) \cdot \overline{Q(t)} = Q(t-0) \cdot \overline{P(t)} \cdot \overline{C(t)} \end{cases} \tag{7.1}$$

and respectively

$$C(t) \cdot (\overline{Q(t-0)} \cdot \overline{Q(t)} \cup Q(t-0) \cdot Q(t)) \cdot (\overline{P(t)} \cdot \overline{D(t)} \cup P(t) \cdot D(t)) \cup \tag{7.2}$$
$$\cup \overline{C(t)} \cdot (\overline{Q(t)} \cdot \overline{P(t-0)} \cdot \overline{P(t)} \cup Q(t) \cdot P(t-0) \cdot P(t)) = 1$$

D, C, P, Q are signals, called: the data input D, the clock input C, the next state P and the state Q. We observe that the equations of the D flip-flop represent the special case of edge triggered RS flip-flop when $R = \overline{S \cdot C}$ and S was noted with D. The D flip-flop has the state Q constant except for the time instants when $C(t-0) \cdot \overline{C(t)} = 1$; then $Q(t) = D(t-0)$.

8 JK flip-flop

The equivalent statements:

$$\begin{cases} \overline{P(t-0)} \cdot P(t) = \overline{P(t-0)} \cdot J(t) \cdot \overline{Q(t)} \cdot C(t) \\ P(t-0) \cdot \overline{P(t)} = P(t-0) \cdot K(t) \cdot Q(t) \cdot C(t) \\ \overline{Q(t-0)} \cdot Q(t) = \overline{Q(t-0)} \cdot P(t) \cdot \overline{C(t)} \\ Q(t-0) \cdot \overline{Q(t)} = Q(t-0) \cdot \overline{P(t)} \cdot \overline{C(t)} \end{cases} \tag{8.1}$$

and

$$C(t) \cdot (\overline{Q(t-0)} \cdot \overline{Q(t)} \cup Q(t-0) \cdot Q(t)) \cdot (P(t) \cdot J(t) \cdot \overline{Q(t)} \cup \overline{P(t)} \cdot K(t) \cdot Q(t) \cup$$
$$\cup (\overline{P(t-0)} \cdot \overline{P(t)} \cup P(t-0) \cdot P(t)) \cdot (\overline{J(t)} \cdot \overline{K(t)} \cup \overline{J(t)} \cdot \overline{Q(t)} \cup \overline{K(t)} \cdot Q(t))) \cup \tag{8.2}$$
$$\cup \overline{C(t)} \cdot (\overline{Q(t)} \cdot \overline{P(t-0)} \cdot \overline{P(t)} \cup Q(t) \cdot P(t-0) \cdot P(t)) = 1$$

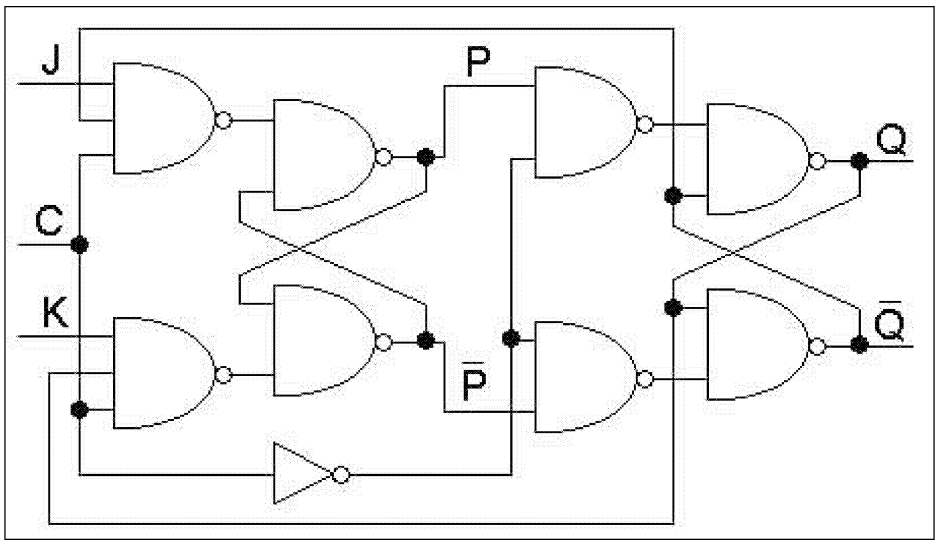

Figure 15: The JK flip-flop circuit

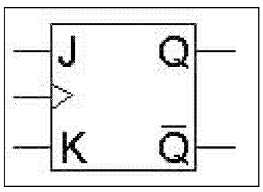

Figure 16: The symbol of the JK flip-flop

are called the equations of the JK flip-flop. J, K, C, P, Q are signals: the J input, the K input, the clock input C, the next state P and the state Q. The first two equations of (8.1) (modeling the master latch) coincide with the first two equations of the edge triggered RS flip-flop where $S(t) = J(t) \cdot \overline{Q(t)}$, $R(t) = K(t) \cdot Q(t)$ and the last two equations of (8.1) (modeling the slave latch) coincide with the last two equations of the edge triggered RS flip-flop. We observe that the conditions of admissibility of the inputs of the master and of the slave latch are fulfilled. To be compared (8.2) and (6.2). The JK flip-flop is similar with the edge triggered flip-flop, for example Q changes value only when $C(t-0) \cdot \overline{C(t)} = 1$. Let $C(t) = 1$; because $Q(t) = Q(t-0)$ i.e. Q is constant, in the reunion

$$P(t) \cdot J(t) \cdot \overline{Q(t)} \cup \overline{P(t)} \cdot K(t) \cdot Q(t) \cup$$

$$\cup (\overline{P(t-0)} \cdot \overline{P(t)} \cup P(t-0) \cdot P(t)) \cdot (\overline{J(t)} \cdot \overline{K(t)} \cup \overline{J(t)} \cdot \overline{Q(t)} \cup \overline{K(t)} \cdot Q(t))$$

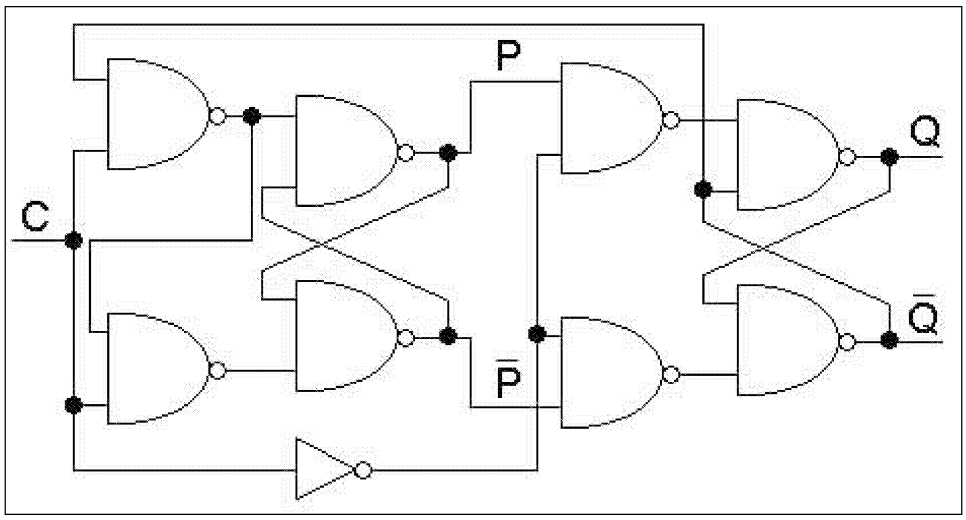

Figure 17: The T flip-flop circuit

only one of $P(t)\cdot J(t)\cdot\overline{Q(t)}$, $\overline{P(t)}\cdot K(t)\cdot Q(t)$ can be 1, thus P changes value at most once and this was not the case at the edge triggered RS flip-flop. Let's make now in the equations of the D flip-flop $D(t) = J(t)\cdot\overline{Q(t)}\cup\overline{K(t)}\cdot Q(t)$. We get

$$\begin{aligned} C(t)\cdot(\overline{Q(t-0)}\cdot\overline{Q(t)}\cup Q(t-0)\cdot Q(t))\cdot(P(t)\cdot J(t)\cdot\overline{Q(t)}\cup\overline{P(t)}\cdot K(t)\cdot Q(t)\cup \\ \cup\overline{P(t)}\cdot\overline{J(t)}\cdot\overline{Q(t)}\cup P(t)\cdot\overline{K(t)}\cdot Q(t))\cup \\ \cup\overline{C(t)}\cdot(\overline{Q(t)}\cdot\overline{P(t-0)}\cdot\overline{P(t)}\cup Q(t)\cdot P(t-0)\cdot P(t)) = 1 \end{aligned} \tag{8.3}$$

Equations (8.2) and (8.3) have similarities and sometimes the equation of the JK flip-flop is considered to be (8.3).

9 T flip-flop

The next equivalent statements:

$$\begin{cases} \overline{P(t-0)}\cdot P(t) = \overline{P(t-0)}\cdot\overline{Q(t)}\cdot C(t) \\ P(t-0)\cdot\overline{P(t)} = P(t-0)\cdot Q(t)\cdot C(t) \\ \overline{Q(t-0)}\cdot Q(t) = \overline{Q(t-0)}\cdot P(t)\cdot\overline{C(t)} \\ Q(t-0)\cdot\overline{Q(t)} = Q(t-0)\cdot\overline{P(t)}\cdot\overline{C(t)} \end{cases} \tag{9.1}$$

respectively

$$C(t)\cdot(\overline{Q(t-0)}\cdot\overline{Q(t)}\cdot P(t)\cup Q(t-0)\cdot Q(t)\cdot\overline{P(t)})\cup \tag{9.2}$$

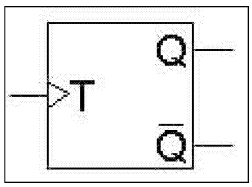

Figure 18: The symbol of the T flip-flop

$$\cup\overline{C(t)} \cdot (\overline{Q(t)} \cdot \overline{P(t-0)} \cdot \overline{P(t)} \cup Q(t) \cdot P(t-0) \cdot P(t)) = 1$$

are called the equations of the T flip-flop. C, P, Q are signals: the clock input, the next state and the state. The conditions of admissibility of the inputs are fulfilled for the first two and for the last two equations from (9.1) (the master and the slave latch). At each falling edge $C(t-0) \cdot \overline{C(t)} = 1$ of the clock input, the state Q of the T flip-flop toggles to its complementary value, otherwise it is constant. The equations of the T flip-flop represent the next special cases: in the equations of the edge triggered RS flip-flop, $S(t) = \overline{Q(t)}, R(t) = Q(t)$; in the equations of the D flip-flop $D(t) = \overline{Q(t)}$; in the equations of the JK flip-flop (any of (9.2), (9.3)) $J(t) = 1, K(t) = 1$.

10 Conclusions

Digital electrical engineering is a non-formalized theory, where the latches are fundamental circuits. In our work we have given the general form of the equations that model the ideal latches, together with the theorem that characterizes the existence and the uniqueness of the solution. Furthermore, we have shown the manner in which this system of equations is particularized in the case of the most well known latches and flip-flops.

The bibliography dedicated to the latches is rich and descriptive (non-formalized). We have indicated at the references a source of inspiration that has created some order in our thoughts.

A possibility of continuing the present ideas is that of considering models of inertial latches, for example we can replace (1.1) with

$$\begin{cases} \overline{x(t-0)} \cdot x(t) = \overline{x(t-0)} \cdot \bigcap\limits_{\xi \in [t-d,t)} u(\xi) \\ x(t-0) \cdot \overline{x(t)} = x(t-0) \cdot \bigcap\limits_{\xi \in [t-d,t)} v(\xi) \\ \bigcap\limits_{\xi \in [t-d,t)} u(\xi) \cdot \bigcap\limits_{\xi \in [t-d,t)} v(\xi) = 0 \end{cases}$$

where $d > 0$. We remark that this model replaces u (v) with $\bigcap_{\xi \in [t-d,t)} u(\xi)$ (with $\bigcap_{\xi \in [t-d,t)} v(\xi)$) meaning that the 1 value of u (of v) continues to produce the switch of x from 0 to 1 (from 1 to 0), but this happens only if it is persistent, i.e. if it lasts at least d time units.

References

[1] Ken Bigelow, www.play-hookey.com, 1996, 2000-2002